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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,806	02/27/2004	Denis Cottin	S1022.81125US00	5628

23628 7590 03/24/2005

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/789,806	COTTIN ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 8-11, 13* is/are rejected.

7)☒ Claim(s) *6,7 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed July 26, 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. The Manetakis reference has not been considered because applicant did not provide page 1091 of the reference.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 is indefinite because the claim is misdescriptive. There is no antecedent basis for the third and fourth transistors. The first line of the last paragraph that begins "are PMOS transistors" is unclear. What are the applicant calling PMOS transistors? It appears to the examiner that this paragraph was taken from claim 8 and inserted into claim 13, which has created the indefiniteness and the antecedent basis problems. Correction or clarification is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al. (U.S. Patent No. 5,049,653).

In reference to claim 2 Smith discloses in Figure 2 an interface circuit comprising one or two input branches (19, 13, 11 and 12, 14, 20) and one output branch (15, 16, 17, 18), each branch being connected between upper and lower supply terminals, each input branch comprising a transistor (11, 12) having its control electrode connected to the input of the interface circuit one of the two other electrodes of the transistor being connected to one of the supply terminals (+VCC, -VCC), a current source (19, 20), being placed between the other one of the supply terminals and an intermediary node connected to the last transistor electrode, at least one of the two input branches comprising one or several diodes (13, 14) connected between the intermediary node and the last transistor electrode of a considered branch, the output branch (15, 16, 17, 18) comprising two complementary transistors (17, 18), having their control electrodes connected to the intermediary nodes of one of the input branches or to the circuit input, one of the electrodes of each of the complementary transistors being connected to the circuit output (VOUT), the last electrode of each of the transistors being connected to a supply terminal (+VCC, -VCC), see column 2, lines 63-65.

In reference to claim 9, the limitations are seen to be design choices dependent on the environment and desired outcome. Furthermore Smith discloses in column 9, lines 19-31 that it is well known in the art that with only slight modifications it is clear to tone skilled in the art that other types of transistors (such as CMOS transistors) may be used. The same applies to claim 10.

In reference to claim 11, Smith discloses in Figure 2 that the transistors are bipolar transistors, the control electrode of a transistor being its base, the two other electrodes being its emitter and collector.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki (JP 2002-044936) in view of Saller et al. (U.S. Patent No. 4,780,689).

In reference to claim 1, Kawasaki discloses in Figure 1 a charge pump circuit comprising first and second transistors of a first type (MP1, MP4), controlled by first complementary signals (PU, NU), third and fourth transistors of a second type (MN1, MN4), controlled by second complementary signals (PD, ND), a first current source (MP2) being placed between a higher voltage terminal (VCC) and a first electrode of the first and second transistors (MP1, MP4), a second current source (MN2) being placed between a lower voltage terminal (gnd) and a first electrode of third and fourth

transistors (MN1, MN4), the second electrodes of the first and third transistors (MP1, MN1) being connected to the circuit output, the second electrodes of second and fourth transistors (MP4, MN4) being connected to a reference node, the circuit output being connected to the input of an interface circuit (B1), the output of the interface circuit (B1) being connected to the reference node. Kawasaki does not disclose that the interface circuit comprises two input branches and one output branch, each branch being connected between upper and lower supply terminals, each input branch comprising a transistor, having its control electrode connected to the input of the interface circuit, one of the two other electrodes of the transistor being connected to one of the supply terminals, a current source, being placed between the other one of the supply terminals and an intermediate node connected to the last transistor electrode, the output branch comprising two complementary transistors, having their control electrodes connected to the intermediary nodes of the two input branches, one of the electrodes of each of the complementary transistors being connected to the interface circuit output, the last electrode of each of the transistors being connected to a supply terminal. Saller discloses in Figure 3 a buffer circuit 4 comprising two input branches (20, 30 and 21, 31) and one output branch (24, 25, 26, 27), each branch being connected between upper and lower supply terminals, each input branch comprising a transistor (30, 31), having its control electrode connected to the input of the interface circuit (2), one of the two other electrodes of the transistor being connected to one of the supply terminals (+Vcc, -Vcc), a current source (20, 21), being placed between the other one of the supply terminals and an intermediate node connected to the last transistor electrode,

the output branch comprising two complementary transistors (24, 25), having their control electrodes connected to the intermediary nodes of the two input branches (20, 30 and 21, 31), one of the electrodes of each of the complementary transistors (24, 25) being connected to the interface circuit output (1), the last electrode of each of the transistors being connected to a supply terminal (6, 7). It would have been obvious to one skilled in the art at the time of the invention that the buffer/interface circuit of Saller could be used in place of the buffer/interface circuit (B1) of Kawasaki for the advantage of providing additional gain of transistors 30 and 31 to buffer terminal 1, as disclosed by Saller in column 3, lines 26-29.

In reference to claim 3, Saller does not disclose that the transistors are CMOS transistors. However, it is considered well known to those having skill in the art that the bipolar transistors of Saller can be replaced with other types of transistors including CMOS types having the same connections as called for in the claim. The same applies to claim 4, wherein the limitation is considered to be a design choice dependent on the environment and the desired outcome. The same also applies to claim 8, wherein the PMOS and NMOS transistors of the first and second branch are seen to be equivalent to the PNP and NPN transistors (30, 31), respectively; and the NMOS and PMOS transistors of the output branch are equivalent to the NPN and PNP transistors (24, 25), respectively.

In reference to claim 5, Kawasaki does not disclose that the transistors are bipolar transistors. However, it is considered well known to those having skill in the art

that the MOS transistors of Kawasaki can be replaced with other types of transistors including bipolar types.

Allowable Subject Matter

8. Claims 6-7 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is an examiner's statement of reasons for allowance: Claims 6 and 12 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the interface circuit has a single input branch wherein the gate of the PMOS transistor (P12) of the output branch being connected to the circuit input (E_{10}) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 7 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the interface circuit includes a second diode (N23) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

March 16, 2005

Terry D. Cunningham
Primary Examiner